second means of interrupt processing for managing communication with the CPU of interrupts of a second interrupt type;

means for routing interrupts of the first interrupt type to the second interrupt processing means;

means for managing interrupts of the first interrupt type by the second interrupt processing means exclusive of the first interrupt processing means.

REMARKS

In response to the above-identified Office Action, Applicant amends the application and seeks reconsideration thereof. In this response, Applicant amends claims 1-13 and 15. Applicant does not add any claims. Applicant cancels claim 14. Applicant does not add any new claims . Accordingly, claims 1-13 and 15 are pending.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attachment is captioned "Version With Markings To Show Changes Made."

I. Claims Rejected Under 35 U.S.C. § 102(b)

Claims 1, 5 and 15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5, 619,706 issued to Young (hereinafter "Young"). Applicants respectfully disagree for the following reasons.

It is axiomatic that to anticipate a claim, each element of the claim must be disclosed in a single reference. Claim 1 includes the elements of "re-routing the initialization data to a second interrupt controller." Young does not teach these elements of claim 1. Rather, Young teaches a switching apparatus for passing interrupts from a first interrupt handling circuit 375 to a second interrupt handling circuit 350 under defined circumstances. The system of Young enables the second interrupt handling circuit 350 to be able to handle a greater number of IRQ lines than it

was actually designed to handle by passing interrupts that must be handled by the second interrupt handler circuit 350 from the first interrupt handler circuit 375 to the second. The first interrupt handler circuit manages IRQ lines labeled "IRQ2" and directly handles those lines when it is not necessary to pass them to the other circuit. See Young col. 5 line 55 – col. 6 line 4. Thus, Young teaches re-routing interrupts not re-routing initialization information for an interrupt handling circuit. The Examiner has failed to identify any part of Young that teaches re-routing the initialization information of an interrupt handling circuit. In fact, Young teaches away from re-routing initialization information because both of the interrupt handling circuits remain functional, each handling interrupts under defined circumstances. Thus, both circuits must be properly initialized to handle interrupts and re-routing the initialization information would be inappropriate. Thus, Young does not teach each of the elements of claim 1. Accordingly, reconsideration and withdrawal of the anticipation rejection of claim 1 are requested.

In regard to claim 5, this claim includes the elements of "re-routing initializing data to a second interrupt controller." Thus, for the reasons mentioned in regard to claim 1 this claim is not anticipated by Young. Accordingly, reconsideration and withdrawal of the anticipation rejection of claim 5 are requested.

In regard to claim 15, this claim includes the element of a "means for managing interrupts of the first type by the second interrupt processing means exclusive of the first interrupt processing means." Young does not teach this element of claim 15. Rather, Young teaches a first interrupt handling circuit that forwards interrupts to a second interrupt handling circuit, as discussed above. Thus, neither interrupt handling circuit of Young can operate exclusive of the other circuit to process interrupts intended for the other circuit. Therefore, Young does not teach

each element of claim 15. Accordingly, reconsideration and withdrawal of the anticipation rejection of claim 15 are requested.

II. Claims Rejected Under 35 U.S.C. § 103

Claims 2-4 and 6-14 stand rejected under 35 U.S.C. § 103 as unpatentable over Young as applied to claims 1, 5 and 15 and in view of U.S. Patent No. 5,987,538 issued to Tavallaei et al (hereinafter "Tavallaei"). Applicants respectfully disagree for the following reasons.

In order to establish a *prima facie* case of obviousness, the Examiner must show that the cited references, combined, teach or suggest each element of a claim. In regard to claims 2-4 and 6-8, these claims depend from independent claims 1 and 5 and incorporate the limitations thereof. Thus, for the reasons mentioned above, Young does not teach each of the elements of claims 1 and 5, namely, re-routing the initialization data. Further, Tavallaei does not cure the defects of Young. The Examiner has not identified any part of Tavallaei that teaches or suggest the re-routing of initialization data. Thus, the cited references do not teach or suggest each of the elements of independent claims 1 and 5. Accordingly, reconsideration and withdrawal of the obviousness rejection of dependent claim 2-4 and 6-8 are requested.

Claim 9 includes many of the same elements as independent claim 15, including the elements of the second interrupt controller handling the interrupts of the first controller exclusive of the first controller. See claim 9, lines 16 and 17. Thus, for the reasons mentioned in regard to claim 15, claim 9 is not obvious over the cited references. Accordingly, reconsideration and withdrawal of the obviousness rejection of claim 9 are requested.

In regard to claims 10-13 these claims depend from independent claim 9 and incorporate the limitations thereof. Thus, at least for the reasons mention in regard to claim 9, these claims are not obvious over Young in view of Tavallaei. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 10-13 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-13 and 15 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: November 26, 2002

By: _____
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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231, on November 26, 2002.

_____
Jean Svoboda November 26, 2002

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A method comprising:

[trapping] sending initializing data [of] related to at least a first interrupt type to a first interrupt controller;

re-routing the initializing data [of] related to at least the first interrupt type to a second interrupt controller; and

configuring the second interrupt controller to manage interrupts of at least the first interrupt type.

2. (Amended) The method of claim 1, [wherein trapping initializing data of a first interrupt type] further compris[es]ing:

configuring a system management interrupt to recognize initializing data [of] related to at least the first interrupt type.

3. (Amended) The method of claim 1, further comprising:

configuring a system management interrupt to recognize initializing data related to at least the first interrupt type; and

re-routing initializing data to the second interrupt controller starting from a first command word,

wherein initializing data [of] related to at least the first interrupt type comprises a plurality of command words [and] including the [a] first command word that begins the initializing of the first interrupt controller. [configuring a system management interrupt to recognize initializing data of a first interrupt type and re-route initializing data to the second interrupt controller from the first command word.]

4. (Amended) The method of claim 1, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises an advanced programmable interrupt controller.

5. A machine readable storage media containing executable program instructions which when executed cause a digital processing system to perform a method comprising:

[trapping] sending initializing data [of] related to at least a first interrupt type to a first interrupt controller;

re-routing initializing data [of] related to at least [a] the first interrupt type to a second interrupt controller; and

configuring the second interrupt controller to manage interrupts of the first interrupt type.

6. The media of claim 5, [wherein trapping initializing data of a first interrupt type] further compris[es]ing:

configuring a system management interrupt to recognize initializing data [of] related to at least [a] the first interrupt type.

7. The media of claim 5, further comprising:

configuring a system management interrupt to recognize initializing data related to at least the first interrupt type; and

re-routing initializing data to the second interrupt controller starting from a first command word,

wherein initializing data [of] related to at least the first interrupt type comprises a plurality of command words [and] including [a] the first command word that begins the initializing of the first interrupt controller. [configuring a system management interrupt to recognize initializing data of a first interrupt type and re-route initializing data to the second interrupt controller from the first command word.]

8. The media of claim 5, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises an advanced programmable interrupt controller.

9. A system comprising:

a central processing unit (CPU);

a first bus coupled to the CPU;

a first interrupt controller, coupled to the first bus, operable to manage communication with the CPU of interrupts of a first interrupt type;

a second bus coupled to the CPU;

a second interrupt controller, coupled to the second bus and to the first interrupt controller, operable to manage communication with the CPU of interrupts of a second interrupt type; and

a memory coupled to the second interrupt controller comprising a computer-readable medium having a computer-readable program embodied therein for directing operation of the system, the computer-readable program comprising:

instructions for managing interrupts of the first interrupt type by the second interrupt controller, exclusive of the first interrupt controller.

10. The system of claim 9, wherein the computer-readable program further comprises:

instructions for [trapping] sending initializing data [of] related to at least a first interrupt type to the first interrupt controller;

instructions for re-routing initializing data [of] related to at least [a] the first interrupt type to the second interrupt controller; and

instructions for configuring the second interrupt controller to manage interrupts of the first interrupt type.

11. The system of claim 10, wherein the instructions for [trapping] re-routing initializing data comprise:

instructions for configuring a system management interrupt to recognize initializing data [of a] related to at least the first interrupt type.

12. The system of claim 10, wherein initializing data [of] related to at least the first interrupt type comprise a plurality of command words and a first command word begins the initializing of the first interrupt controller, and the computer-readable program comprises instructions for configuring a system management interrupt to recognize initializing data [of] related to at least [a] the first interrupt type and re-route initializing data to the second interrupt controller from the first command word.

13. The system of claim 9, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises an advanced programmable interrupt controller.

15. A system comprising:

a central processing unit (CPU);

first means of interrupt processing for managing communication with the CPU of interrupts of a first interrupt type;

second means of interrupt processing for managing communication with the CPU of interrupts of a second interrupt type;

means for routing interrupts of the first interrupt type to the second interrupt processing means;

means for managing interrupts of the first interrupt type by the second interrupt processing means exclusive of the first interrupt processing means.